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B.Tech. (Sem. - 6th)

DIGITAL SIGNAL PROCESSING

SUBJECT CODE : EC-308

Paper ID : [A0321]

[Note: Please fill subject code and paper ID on OMR]

Time : 03 Hours

Maximum Marks : 60

Instruction to Candidates:

- 1) Section - A is **Compulsory**.
- 2) Attempt any **Four** questions from Section - B.
- 3) Attempt any **Two** questions from Section - C.

Section - A

(10 × 2 = 20)

- Q1)** a) What is the disadvantage of using DSPs if signal with large bandwidth are involved?
- b) What is scaling of discrete time signals?
- c) What is the difference between static and dynamic discrete time signals?
- d) Describe linearity property of Z transform.
- e) Define Circular symmetric of a sequence in DFT.
- f) What is the computational advantage of FFT?
- g) What is the basic difference between cascade form and direct form structures for FIR systems?
- h) In what cases FIR filters will be preferred over IIR filters?
- i) What will happen if length of windows is increased in design of FIR filters?
- j) Write the basic difference between ADSP and TMS series of processors.

Section - B

(4 × 5 = 20)

Q2) Describe basic elements of DSP systems with block diagram.

Q3) Compute convolution of $y(n)$ of the signals

$$X(n) = \begin{cases} \alpha^n, & -3 \leq n \leq 5 \\ 0, & \text{elsewhere} \end{cases}$$

$$h(n) = \begin{cases} 1, & 0 \leq n \leq 4 \\ 0, & \text{elsewhere} \end{cases}$$

Q4) Find Z-transform of the following discrete time sequences

$$X(n) = \sin(n\omega T), \quad n = 0, 1, \dots$$

Q5) A finite duration sequence of length L is given as

$$X(n) = \begin{cases} 1, & 0 \leq n \leq L-1 \\ 0, & \text{otherwise} \end{cases}$$

Determine N -point DFT of this sequence for $N \geq L$.

Q6) Discuss DIT and DIF algorithms and also compare the two algorithms.

Section - C

(2 × 10 = 20)

Q7) (a) Describe Cascade form structure for FIR system.

(b) Discuss quantization of filter coefficients in design of IIR and FIR filter.

Q8) Discuss design of FIR filter using window method. Also compare design using Kaiser and Hanning Windows.

Q9) (a) Why frequency transformation in analog domain is done? Discuss in detail.

(b) Discuss architecture of ADSP processor using a block diagram.

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