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Total No. of Questions : 09] [Total No. of Pages : 02

Paper ID [A0330]

(Please fill this Paper ID in OMR Sheet)

B.Tech. (Sem. - 7th/8th)

VLSI DESIGN AND TECHNOLOGY (EC - 406)

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) *(10 × 2 = 20)*

a) What do you understand by an entity? Explain.

b) Explain the difference between concurrent and sequential programming.

c) What is the difference between GAL and PAL?

d) Explain the 'Generic' statement in VHDL language.

e) Explain the importance of IEEE library in VHDL.

f) Name any two synthesis tools for digital systems.

g) What is a process in VHDL? Explain with example.

h) What is the importance of STD_ LOGIC in VHDL language.

i) What is the difference between a CPLD and an FPGA implementation.

j) Define the role of a compiler in VHDL.

Section - B

(4 × 5 = 20)

Q2) Write a VHDL program to design a 2-bit comparator circuit.

Q3) Explain the internal architecture of an FPGA.

Q4) Explain with suitable examples the use of CASE statement.

Q5) Design a BCD to gray code converter using VHDL language.

Q6) Write a data flow model for 4 to 16 decoder.

Section - C

(2 × 10 = 20)

Q7) Design and implement a simple microcomputer system using VHDL.

Q8) Implement the following boolean function

$F(A,B,C,D,E) = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E} + ABCDE + \overline{A}B\overline{C}D\overline{E}$.

Q9) Write short notes on the following :

(a) CPLD Architecture.

(b) Simulation of sequential circuits.