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Total No. of Questions : 09] [Total No. of Pages : 02

B.Tech. (Sem. - 7th/8th)

VLSI DESIGN & TECHNOLOGY

SUBJECT CODE : EC - 406

Paper ID : [A0330]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory.**
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) *(10 × 2 = 20)*

a) Name the different EDA (electronic design automation) tools available for synthesising and simulating digital systems.

b) How do signed and unsigned data types in VHDL differ from each other?

c) What is operator overloading?

d) Explain : Signal, variable.

e) What is the difference between a process and a function?

f) Sketch a dot diagram for a 2-input XOR using a ROM.

g) What is the difference between concurrent and sequential statement?

h) What are the different sections of a VHDL code?

i) How is programming and erasing of a UV-EPROM done?

j) Describe the structure of a package.

Section - B

(4 × 5 = 20)

Q2) Explain the inertial delay and transport delay in behavioral modelling. Also, give the delay model for each of these.

Q3) How can IF, CASE and LOOP statements be used to control the flow of execution within a model?

Q4) Write the 4-bit shift register VHDL sequential code using the IF statement.

Q5) Draw a basic PAL circuit having four-inputs, eight product terms and one active-low combinational output. Draw fuses on your diagram to realize the following Boolean expression :

$$\overline{F} = \overline{A}B\overline{C} + \overline{B}CD + \overline{A}CD + A\overline{C}D$$

Q6) Using only concurrent statements, design the 8-bit unsigned adder of Fig 1.

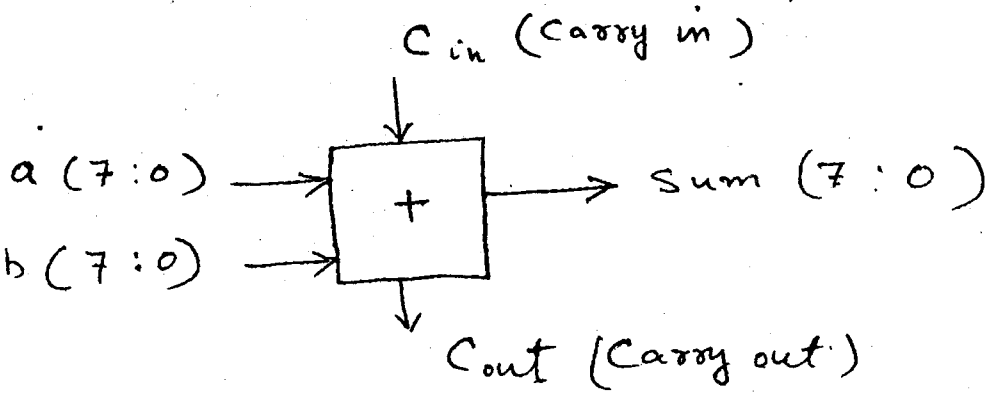

Fig. 1

Section - C

(2 × 10 = 20)

Q7) Write the VHDL code for a serial-parallel multiplier circuit.

Q8) What is meant by CPLD and FPGA? Explain their architecture.

Q9) Design a 4-bit BCD updown counter using VHDL sequential code.

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