VLSI Design and Technology
(EC-406, Dec-2007)

Note: Section A is compulsory. Attempt any four questions from Section-B and any two from Section-C.

Section-A

1. a) What is the difference between simulation and synthesis?
   b) What is SUBTYPING used for?
   c) Create the use data type DAYS and design it the values: MON, TUE, WED, THU, FRI, SAT and SUN.
   d) What is meant by instantiating a component?
   e) What is the prime use if signals? Quote suitable example.
   f) How does procedure differ from functions?
   g) Create the architecture block for the 3-input XOR gate and Add a 25 ns inertial delay to the XOR assignment statement.
   h) Write a function that returns the sum of two 8-bit words.
   i) What is difference between stud_logic_vector and std_ulogic_vector?
   j) Write a statement thet will allow a design o access all the contents of IEEE ARITH library.

Section-B

2. Draw the schematic diagram of 4-bit full adder and write down its structural modeling.
3. Write down VHDL code for binary to 7 segment display.
4. Write about the concept of overloading with the help of example.
5. Write a counter model with a clock input clk of type bit, and an output q of type integer. The behavioral architecture body should contain a process that declares a count variable initialized to zero. The process should wait for changes on clk. When clk changes to '1' the process should increment the count and assign its value to the output port.
6. Generate the "clk1" and "clk2" waveforms for the following two process statements. Both the "clk1" and "clk2" are signals for the type bit.

```
P1: Process is
Begin
Clk1 <="1" after 5 ns, "0" after 10 ns;
      Wait for 10ns;
End;
P2: Process is
Clk2<='1' after 5 ns;
Clk2<='0' after 10 ns;
Wait for 10ns;
End;
```

Section-C

7. Develop a behavioral model of a RAM with generic constants governing the read access time, minimum write time, the address port and the data port width.
8. Discuss the 8-bit serial to parallel and parallel to serial shift register and write code for the same.
9. Write short notes on:
   (a) Guarded signals with the help of examples.
   (b) FPGA Vs. CPLD designing.

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