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Total No. of Questions : 09] [Total No. of Pages : 02

Paper ID [EC406]

(Please fill this Paper ID in OMR Sheet)

MAY-08

B.Tech. (Sem. - 7th/8th)

VLSI DESIGN & TECHNOLOGY (EC - 406)

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) *(10 × 2 = 20)*

a) What is the difference between a entity and an architecture declaration.

b) Which is better and why? Data flow modelling or behavioural modelling.

c) Explain the use of WAIT statement with examples.

d) What is the difference between a library and a package? Explain.

e) What is over loading? Explain.

f) What is the difference between a CPLD and a FPGA implementation.

g) What do you understand by PEEL? Explain.

h) What are the main features of a structural model in VHDL language.

i) Explain the Generic statement in VHDL language.

j) Define the role of a compiler in VHDL.

Section - B

(4 × 5 = 20)

Q2) Design a 3 to 8 decoder using behavioural VHDL modelling.

Q3) Design an 8-bit shift register using VHDL

Q4) Explain the difference between a ROM implementation and a PLA implementation with the help of suitable examples.

Q5) Explain the use of CASE statement using examples.

Q6) Design a BCD to Excess - 3 code converter using VHDL language.

Section - C

(2 × 10 = 20)

Q7) Design a simple 4-bit ALU (Arithmetic logic unit) using VHDL.

Q8) Design a 4-bit Jhonson counter using VHDL language.

Q9) Write short notes on the following:

(a) Resolution functions

(b) Implementation of $F(A,B,C) = \overline{A}B\overline{C} + ABC + A\overline{B}C$ using VHDL.