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B.Tech. (Sem. - 7th / 8th)

VLSI DESIGN AND TECHNOLOGY

SUBJECT CODE : EC - 406

Paper ID : [A0330]

[**Note :** Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) *(10 x 2 = 20)*

a) What is the difference between inertial and transport delay. Give examples of each?

b) What is the logic equivalent of CASE and IF ELSE statement?

c) List the various signal attributes.

d) What are 3 levels of architecture description?

e) What are advantages of designing?

f) What are the different arithmatic and logic operators? List them based on the priority.

g) Write a behavioral architecture code for a 4 bit tristate bus.

h) What is top down design methodology? Give example.

i) What are the different logic levels available in standard logic type?

j) How is generic statement useful in VHDL code.

Section - B

(4 x 5 = 20)

Q2) Enumerate the differences between procedures and function. Explain with suitable example.

Q3) Design a 3-8 bit decoder and write suitable VHDL code for it.

Q4) Write VHDL code for full subtractor using logic equations. Using this as a component write VHDL code for 4 bit subtractor circuit.

Q5) The following state table is implemented using a ROM and 2 D flip flops. (falling edge triggered).

Q_1	Q_2	$Q_1^+ Q_2^+$		$Q_1^+ Q_2^+$		Z	
		x = 0		x = 1		x = 0	x = 1
0	0	0	1	1	0	0	1
0	1	1	0	0	0	1	1
1	0	0	0	0	1	1	0

(a) Draw block diagram.

(b) Write VHDL code that describes the system. Assume the ROM has a delay of 10 ns and each D flip flop has propagation delay of 15 ns.

Q6) Write short notes on PLA's, GAL, PEEL. List advantages of using FPGA's.

Section - C

(2 x 10 = 20)

Q7) What is overloading concept? Explain with a example.

Q8) (a) Design and write a VHDL code for 4 to 1 MUX using behavioral and data flow architecture description.

(b) Design a 3 bit up-down counter and write VHDL code for it.

Q9) (a) Write a VHDL code for a 3 by 3 matrix multiplication using arrays for input vectors definition.

(b) Design a microcomputer that performs various arithmatic and logical operation on bit vectors.